

FORM PTO 609
(REV. 8-83)U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO.

SERIAL NO.

HARI-0611

08/407,916

APPLICANT

Eliyahou Harari et al.

FILED

March 21, 1995

GROUP

2511

INFORMATION DISCLOSURE STATEMENT

Use several sheets if necessary)

U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
<i>JS</i>	A1	4 0 9 9 0 6 9	7/4/78	Cricchi et al.			
<i>JS</i>	A2	4 9 3 1 9 9 7	6/5/90	Mitsuishi et al.			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

<i>JS</i>	✓ B1	Colin S. Bill, et al.; A TEMPERATURE- AND PROCESS- TOLERANT 64K EEPROM, 1985, pp. 979-985
<i>JS</i>	✓ B2	Intel Corporation, 27F256 256K (32K x 8) CMOS FLASH MEMORY, DATA SHEET, May 1988, pp. 1-21
<i>JS</i>	✓ B3	SEEQ Technology Incorp., 48F512 512K FLASH EEPROM - PRELIMINARY DATA SHEET, October 1988, pp. 2-1 - 2-24

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J S P O P E K	A1	3	8	9	5	3	6	0	7/15/75	Cricchi et al.			
	A2	3	8	9	8	6	3	2	8/5/75	Spencer, Jr.			
	A3	3	9	0	6	4	5	5	9/16/75	Houston et al.			
	A4	3	9	1	4	7	5	0	10/21/75	Hadden, Jr.			
	A5	4	0	0	5	3	8	9	1/25/77	Penzel			
	A6	4	0	4	4	3	3	9	8/23/77	Berg			
	A7	4	0	5	8	7	9	9	11/15/77	George et al.			
	A8	4	0	6	4	4	0	5	12/20/77	Cricchi et al.			
	A9	4	0	9	0	2	5	8	5/16/78	Cricchi			
	A10	4	1	1	5	8	5	0	9/19/78	Houston et al.			
	A11	4	1	3	0	8	9	0	12/19/78	Adam			

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		DOCUMENT NUMBER							DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
J S P O P E K	B1	0	2	8	3	2	3	8	9/21/88	Europe			
	B2	5	2	8	7	3	8	✓	1/22/77	Japan			
	B3	5	8	8	6	7	7	7	5/24/83	Japan			
	B4	5	8	2	1	5	7	9	12/15/83	Japan			
	B5	5	8	2	1	5	7	9	12/15/83	Japan			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

J S P O P E K	C1	J.E. Brewer et al., "Block-Oriented Random Access MNOS Memory," National Computer Conference and Exposition, Chicago, May 6-10, 1974, AFIPS Conference Proceedings, Vol. 43
	C2	J.E. Brewer et al., "Low Cost MNOS BORAM," Proceedings of IEEE National Aerospace Electronics Conference, NAECON '77, May 17-19, 1977
	C3	J.R. Cricchi et al., "Nonvolatile Block-Oriented RAM," IEEE International Solid-State Circuits Conference, Feb. 13-15, 1974, Digest of Technical Papers
	C4	Raul-Adrian Cernea et al., "A 1Mb Flash EEPROM," 1989 IEEE International Solid-State Circuits Conference

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[Handwritten signature]	A12 4 1 4 1 0 8 1	2/20/79	Horne et al.			
	A13 4 1 9 3 1 2 8	3/11/80	Brewer			
	A14 4 2 4 1 4 2 4	12/23/80	Dickson et al.			
	A15 4 4 1 2 3 0 9	10/25/83	Kuo			
	A16 4 4 2 8 0 4 7	1/24/84	Hayn et al.			
	A17 4 4 3 3 3 8 7	2/21/84	Dyer et al.			
	A18 4 4 4 9 2 0 3	5/15/84	Adlloch			
	A19 4 4 5 1 9 0 5	5/29/84	Moyer			
	A20 4 4 6 0 9 8 2	7/17/84	Gee et al.			
	A21 4 4 6 8 7 2 9	8/28/84	Schwartz			
	A22 4 5 2 1 8 5 2	6/4/85	Guttag			

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DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
B6 9 4 5 6 9 5	3/14/84	Japan			
B7 5 9 1 6 2 6 9 5	9/13/84	Japan			
B8 5 9 1 8 6 0 1 5	10/22/84	Japan			
B9 6 2 1 8 8 0 9 9	8/17/87	Japan			
B10 6 2 2 8 3 4 9 6	12/9/87	Japan			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

C5	Kenneth L. Short, "Microprocessors and Programmed Logic," second edition. "Ch. 13.2.2 Electrically Erasable Programmable Read Only Memory, EEPROM" Prentice Hall International, 1987
C6	Michael D. Fitzpatrick et al., "MNOS/SOS Memory Using High-Voltage Depletion-Mode CMOS Logic"
C7	J.R. Cricchi et al., "The Drain-Source Protected MNOS Memory Device and Memory Endurance," IEDM Technical Digest, 1973
C8	Virgil Kynett et al., "An In-System Reprogrammable 32Kx8 CMOS Flash Memory," IEEE J. Solid-State Circuits, Vol. 23, No. 5, October, 1988

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A23 A24 A25 A26 A27 A28 A29 A30 A31 A32 A33 A34 A35 A36 A37 A38	A23	4	5	2	1	8	5	3		6/4/85	Gutttag			
	A24	4	5	2	7	2	5	7		7/2/85	Cricchi			
	A25	4	6	4	2	7	9	8		2/10/87	Rao			
	A26	4	6	8	5	0	8	4		8/4/87	Canepa			
	A27	4	7	5	8	9	8	6		7/19/88	Kuo			
	A28	4	7	5	8	9	8	8		7/19/88	Kuo			
	A29	4	7	6	3	3	0	5		8/9/88	Kuo			
	A30	4	7	8	0	8	5	5		10/25/88	Iida et al.			
	A31	4	7	9	6	2	3	5		1/3/89	Sparks et al.			
	A32	4	8	0	5	1	5	1		2/14/89	Terada et al.			
	A33	4	8	1	1	2	9	3		3/7/89	Knothe et al.			
	A34	4	8	1	1	2	9	4		3/7/89	Kobayashi et al.			
	A35	4	8	2	1	2	4	0		4/11/89	Nakamura et al.			
	A36	4	8	3	9	7	0	5		6/13/89	Tigelaar et al.			
	A37	4	8	4	1	4	8	2		6/20/89	Kreifels et al.			
	A38	4	8	6	0	2	2	8		8/22/89	Carroll			

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		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
B11 B12 B13 B14 B15	B11	6 2 2 8 3 4 9 7	12/9/87	Japan			
	B12	6 3 1 8 5 9 6	1/26/88	Japan			
	B13	6 3 1 0 6 9 8 9	5/12/88	Japan			
	B14	6 3 1 8 3 7 0 0	7/29/88	Japan			
	B15	6 3 2 2 5 9 9 9	9/20/88	Japan			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

C9	Denny Cormier, "Erasable/Programmable Solid-State Memories," EDN, pp. 145-154, November 14, 1985
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A39	A39	4	8	6	0	2	6	1		8/22/89	Kreifels et al.			
	A40	4	8	6	0	2	6	2		8/22/89	Chiu			
	A41	4	8	7	8	2	0	3		10/31/89	Arakawa			
	A42	4	8	8	2	6	4	2		11/21/89	Tayler et al.			
	A43	4	8	8	7	2	3	4		12/12/89	Iijima			
	A44	4	9	2	0	4	7	8		4/24/90	Furuya et al.			
	A45	4	9	3	3	9	0	6		6/12/90	Terada et al.			
	A46	4	9	3	9	6	9	0		7/3/90	Momodomi et al.			
	A47	4	9	5	3	1	2	9		8/28/90	Kobayashi et al.			
	A48	5	0	3	3	0	2	3		7/16/91	Hsia et al.			
	A49	5	0	3	6	4	6	0		7/30/91	Takahira et al.			
	A50	5	0	4	3	9	4	0		8/27/91	Harari			
	A51	5	0	5	3	9	9	0		10/1/91	Kreifels et al.			
	A52	5	0	8	4	8	4	3		1/28/92	Mitsuishi et al.			
	A53	5	1	6	8	4	6	5		12/1/92	Harari			
	A54	5	2	6	8	8	7	0		12/7/93	Harari			

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